CLAIMS

What is claimed is:

1. A dynamic random access memory (DRAM) cell providing reading, writing, and storage of a data bit, said cell comprising:

a first transistor having a first source node, a first gate node, and a first drain node; and

a second transistor having a second drain node that is electrically connected to said first drain node, and said second transistor having a second source node and a second gate node.

2. The cell of claim 1 wherein said second source node is electrically floating.

3. The cell of claim 1 wherein said first transistor is a field-effect-transistor (FET) acting as a memory pass gate to read and write said data bit.

4. The cell of claim 1 wherein said second transistor is a FET acting as a memory storage for storing said data bit.

5. The cell of claim 1 wherein said first drain node and said second drain node, connected together, constitute a storage node.

6. The cell of claim 1 further comprising a pulsed voltage driver connected to said second gate node.

7. The cell of claim 1 wherein said first gate node comprises a memory read/write-enable line.

8. The cell of claim 1 wherein said first source node comprises a memory bit line that is written to and read from.

9. The cell of claim 1 wherein said first transistor and said second transistor comprise a memory cell embedded on an ASIC chip using CMOS technology.

10. The cell of claim 1 wherein said second transistor has a first storage capacitance associated with a junction of said second transistor and a second storage capacitance associated with an oxide layer of said second source node to store said data bit.

11. A method for reducing leakage current when storing a data bit in an embedded DRAM cell, said method comprising:

writing a data bit to a DRAM cell during a first time segment;

applying a transistor disabling reference ground potential to a first gate node of a first transistor of said DRAM cell during a second time segment, said second time segment being after said first time segment;

applying a first reference voltage, with respect to said reference ground potential, to a first source node of said first transistor during said second time segment; and

applying a second reference voltage, with respect to said reference ground potential, to a second gate node of a second transistor during at least a portion of said second time segment.

12. The method of claim 11 wherein said writing comprises:

applying a data bit voltage to said first source node of said first transistor during said first time segment;

applying a read/write-enabling voltage level, with respect to said reference ground potential, to said first gate node of said first transistor during said first time segment; and

applying said read/write-enabling voltage level to said second gate node of said second transistor during at least said first time segment.

13. The method of claim 12 wherein said read/write-enabling voltage level is equal to said first reference voltage.

14. The method of claim 12 wherein said read/write-enabling voltage level is more positive than said first reference voltage.

15. The method of claim 11 wherein said second reference voltage is more positive than said first reference voltage.

16. The method of claim 11 wherein a first drain node of said first transistor is electrically connected to a second drain node of said second transistor.

17. The method of claim 11 wherein a second source node of said second transistor is electrically floating.

18. The method of claim 11 wherein said first transistor is a FET acting as a memory pass gate.

19. The method of claim 11 wherein said second transistor is a FET acting as a memory storage.

20. The method of claim 11 wherein said first transistor and said second transistor are embedded on an ASIC chip using CMOS technology.

21. The method of claim 11 wherein said second transistor has a first storage capacitance associated with a junction of said second transistor and a second storage capacitance associated with an oxide layer of a second source node of said second transistor to store said data bit.

22. The method of claim 11 wherein said data bit is represented by a voltage level corresponding to said reference ground potential.

23. The method of claim 11 wherein said data bit is represented by a voltage level that is more positive than said reference ground potential.